**POWER-EFFICIENT DRAM SENSE AMPLIFIER DESIGN USING POWER GATING IN 45NM TECHNOLOGY**

***A Project report submitted to***

**JAWAHARLAL NEHRU TECHONOLOGICAL UNIVERSITY ANANTAPUR,**

**ANANTHAPURAMU**

*in partial fulfilment of the requirements for*

*the award of the degree of*

**BACHELOR OF TECHNOLOGY**

**in**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

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SREE VIDYANIKETHAN ENGINEERING COLLEGE

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**(2021-2025)**

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| **PSO4.** | Apply appropriate techniques, resources, and modern tools to complex engineering systems and processes in the domains of Electronics, Signal Processing,  Communications, and VLSI & Embedded Systems. |

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Certificate

This is to certify that the Project Report entitled

**“Power-Efficient DRAM Sense Amplifier Design Using Power Gating In 45NM Technology ”**

is the bonafide work done and submitted by

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**DECLARATION**

We hereby declare that project report entitled “**POWER-EFFICIENT DRAM SENSE AMPLIFIER DESIGN USING POWER GATING IN 45NM TECHNOLOGY**” being submitted by us for award of degree of Bachelor of Technology in Electronics and Communication Engineering, Jawaharlal Nehru Technological University Anantapur, Anantapuramu is a bonafide record of SREE VIDYANIKETHAN ENGINEERING COLLEGE and has not been submitted to any other courses or university for award of any degree.

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**ABSTRACT**

Power consumption is a critical consideration in the design of memory elements and digital systems within very large scale integration (VLSI) circuits. This study introduces a method for reducing power consumption in DRAM sense amplifiers, termed FSPA-VLSA (Foot Switch PMOS Access Voltage Latch Type Sense Amplifier). By implementing this technique within the open bit architecture of DRAM Cells during read operations, an approximate 81% reduction in overall power consumption has been achieved. Additionally, this proposed circuit offers advantages for low-power VLSI/ULSI design. The circuit has been successfully designed and implemented using Cadence Virtuoso tools at 45nm technology.

**Keywords**—Basic latch type sense amplifier, capacitor, DRAM Cell, FSPA-VLSA

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**CHAPTER 1**

**INTRODUCTION**

**1.1. Overview of the Problem**

The evolution of semiconductor technology has significantly influenced the landscape of computing systems, with dynamic random-access memory (DRAM) emerging as a cornerstone of modern electronics. DRAM serves as the primary memory component in a wide range of devices, including computers, smartphones, and IoT devices, enabling rapid data access and storage. Within the intricate architecture of DRAM cells, the sense amplifier plays a pivotal role in facilitating efficient read operations, thereby enhancing overall system performance. As semiconductor manufacturing processes continue to advance, the design of DRAM sense amplifiers becomes increasingly critical to meet the escalating demands for higher memory density, speed, and energy efficiency.

A comprehensive understanding of DRAM technology is essential to appreciate the significance of sense amplifiers within memory cells. DRAM operates on the principle of storing data as charge in capacitors, with each cell comprising a capacitor and an access transistor. During read operations, the sense amplifier detects and amplifies the small signal difference between the charged and discharged states of the capacitor, enabling accurate retrieval of stored data. Furthermore, the chapter delves into the intricacies of DRAM refresh cycles, addressing the challenges posed by data retention and degradation over time.

A thorough examination of existing DRAM sense amplifier designs provides valuable insights into architectural trends and performance characteristics. Through an extensive literature review encompassing academic research and industrial innovations, various sense amplifier architectures are analyzed based on their speed, power efficiency, noise immunity, and area

footprint. The review highlights the evolution of sense amplifier designs across different technology nodes, shedding light on the strengths and limitations of each approach.

With a solid foundation in DRAM technology and sense amplifier design principles, the thesis outlines clear objectives and methodologies for designing DRAM sense amplifiers using 45nm technology. The design goals prioritize maximizing read speed, minimizing power consumption, and ensuring resilience against process variations. A systematic approach to circuit design, simulation, optimization, and validation is established, leveraging advanced tools and methodologies available in the design ecosystem.

Random-access memory (RAM) stands as a fundamental component of modern computing systems, playing a crucial role in facilitating rapid data access and storage. As a volatile memory type, RAM allows for temporary storage of data and instructions that are actively being used or processed by the CPU (Central Processing Unit). This temporary nature distinguishes RAM from other forms of storage, such as hard disk drives (HDDs) and solid-state drives (SSDs), which retain data even when power is turned off.

**1.2. Types of RAM**

Several types of RAM exist, each offering unique characteristics tailored to specific applications and performance requirements:

**1.2.1. Dynamic Random-Access Memory (DRAM):** DRAM is the most common type of RAM used in computing systems. It stores data in capacitors within memory cells and requires periodic refresh cycles to maintain data integrity. Despite its relatively slower access times compared to other types of RAM, DRAM remains prevalent due to its high storage density and cost-effectiveness.

**1.2.2. Static Random-Access Memory (SRAM):** SRAM differs from DRAM in that it uses latching circuitry to store data, eliminating the need for refresh cycles. This results in faster access times and lower power consumption compared to DRAM, making SRAM well-suited for cache memory and other high-speed applications.

**1.2.3. Synchronous Dynamic Random-Access Memory (SDRAM):** SDRAM synchronizes memory operations with the system clock, allowing for more efficient data transfers compared to asynchronous DRAM. Variants such as DDR (Double Data Rate) SDRAM and DDR4 SDRAM further enhance data throughput by doubling the data transfer rate per clock cycle.

**1.2.4. Non-Volatile RAM (NVRAM):** NVRAM retains data even when power is turned off, blurring the line between traditional RAM and non-volatile storage. Technologies such as Magnetoresistive RAM (MRAM) and Phase-Change RAM (PRAM) offer fast read and write speeds akin to volatile RAM while providing data persistence similar to SSDs and HDDs.

In the realm of digital electronics, particularly within memory design, sense amplifiers stand as indispensable components, playing a pivotal role in enhancing the reliability, speed, and efficiency of memory read operations. These vital circuits serve as the bridge between the intrinsic properties of memory cells and the external data processing units, facilitating the seamless retrieval of stored information in memory arrays.

**1.3. Functionality of Sense Amplifiers**

Sense amplifiers function as the frontline interpreters of the subtle electrical signals emanating from memory cells during read operations. Their primary functions can be elucidated as follows:

**1.3.1. Signal Amplification**: Memory cells store binary data by altering electrical characteristics, such as charge or voltage levels. During read operations, sense amplifiers amplify the weak signals retrieved from memory cells to discern the stored data accurately. This amplification process is crucial for differentiating between different data states, such as "0" and "1," ensuring precise data retrieval.

**1.3.2. Signal Detection and Interpretation:** After amplification, sense amplifiers compare the amplified signals against predetermined thresholds to ascertain the logical state of each memory cell. Employing differential sensing techniques, sense amplifiers discern minute voltage differentials between bitlines, enabling reliable discrimination between different data states.

**1.3.3. Noise Rejection:** Sense amplifiers are engineered to minimize the impact of noise and interference that may distort the retrieved signals. Through sophisticated circuit design and signal processing algorithms, sense amplifiers enhance signal fidelity by mitigating noise, thereby improving the accuracy and reliability of read operations, particularly in noisy environments.

**1.3.4. Speed Enhancement:** Critical to memory performance, sense amplifiers contribute to reducing access times and latency by expediting the amplification and interpretation of signals. Their swift operation ensures rapid data retrieval from memory arrays, optimizing overall system performance, and responsiveness, particularly in high-throughput computing applications.

**1.4. Significance in Memory Systems**

Sense amplifiers hold immense significance in memory systems due to their multifaceted roles in ensuring accurate data retrieval, noise immunity, and high-speed operation. As the interface between memory cells and external processing units, the efficacy of sense amplifiers profoundly impacts the overall performance and reliability of memory systems.

As memory technologies continue to advance, the design and optimization of sense amplifiers remain a focal point for research and development. Emerging trends such as non-volatile memory and three-dimensional memory architectures present new challenges and opportunities for sense amplifier design, necessitating innovative solutions to meet the demands of future memory systems. Therefore, ongoing research endeavors aim to further enhance the efficiency, speed, and reliability of sense amplifiers to address the evolving needs of modern computing applications.

**1.5. Role Of Sense Amplifiers in DRAM**

Sense amplifiers play a critical role in dynamic random-access memory (DRAM) systems, where they are instrumental in the read and write operations of memory cells. In DRAM, memory cells store data in the form of charge, typically representing binary states (0 or 1). Sense amplifiers are deployed to accurately detect and amplify these weak charge signals during read operations, ensuring reliable data retrieval from memory cells.

During read operations in DRAM, sense amplifiers are responsible for detecting and amplifying the charge stored in memory cells. As each memory cell holds a tiny charge representing a data bit, sense amplifiers amplify these signals to a level that can be accurately interpreted as either a logical 0 or 1. This process is crucial for retrieving the correct data from memory cells, and the efficiency of sense amplifiers directly impacts the speed and accuracy of read operations in DRAM systems.

In addition to read operations, sense amplifiers also play a role in write operations in DRAM. When data is to be written to a memory cell, sense amplifiers help in driving the appropriate charge onto the memory cell, ensuring that the desired data is stored accurately. Sense amplifiers assist in the process of writing data to memory cells, contributing to the overall reliability and integrity of the stored information.

Sense amplifiers also contribute to maintaining signal integrity in DRAM systems. They help in mitigating noise and other interferences that may affect the accuracy of read and write operations. By amplifying and accurately detecting charge signals, sense amplifiers enhance the robustness of data retrieval and storage processes in DRAM, improving overall system performance and reliability.

The speed and efficiency of sense amplifiers are critical factors in DRAM systems, where fast access times and high throughput are essential. Sense amplifiers need to operate swiftly and reliably to ensure rapid read and write operations, minimizing access latency and optimizing memory performance. Efficient sense amplifiers contribute to the overall efficiency and responsiveness of DRAM systems, enabling them to meet the demands of modern computing applications.

**CHAPTER 2**

**LITERATURE REVIEW**

**2.1. Dynamic Random Access Memory (DRAM)**

Y. L. Sung-MO Kang, "Dynamic Random Access Memory (DRAM)," in CMOS digital integrated circuits, new delhi, mcgraw hill, 2013, p. 655.

Dynamic Random Access Memory (DRAM) stands as a cornerstone of computing systems, renowned for its fast and efficient memory access capabilities. However, despite its widespread adoption and utility, DRAM technology is not immune to limitations that warrant thorough consideration. One of the foremost challenges associated with DRAM is its inherent volatility. Another significant limitation of DRAM lies in its reliance on refresh cycles to counteract leakage currents that degrade stored charge over time. These refresh cycles, while essential for maintaining data integrity, consume both time and energy, thereby reducing the overall efficiency of DRAM-based systems. The need for frequent refresh operations introduces latency and can impact system performance, particularly in applications with high memory access rates. Additionally, DRAM exhibits relatively high power consumption compared to other memory technologies. The continuous operation required for refresh cycles contributes to this power consumption, making DRAM less energy-efficient, especially in mobile and battery-powered devices where power efficiency is crucial. Furthermore, DRAM is susceptible to various types of errors, including single-bit errors, multi-bit errors, and row hammering. Single-bit errors occur when a bit stored in a DRAM cell flips unintentionally due to external factors such as cosmic radiation or electrical noise. Multi-bit errors can result from the simultaneous occurrence of multiple single-bit errors, leading to data corruption. Row hammering, on the other hand, is a phenomenon where repeated accesses to adjacent rows in DRAM can cause bit flips in neighbouring rows, potentially compromising system security and stability.

**2.2. High Speed Low Power Sense Amplifier Design**

**Arsovski, "High-Speed Low-Power Sense Amplifier Design," 12 NOV,2001**

While significant progress has been made in the development of sense amplifiers to meet the demands of high-speed and low-power memory architectures, several limitations persist in current designs. One of the primary limitations is associated with achieving a balance between speed and power consumption. Sense amplifiers must operate quickly to minimize read access times in memory systems, but this often comes at the expense of increased power consumption. Another limitation lies in the sensitivity and robustness of sense amplifiers to noise and variations in operating conditions. In high-speed memory systems, signal integrity is paramount, and any noise introduced during the sensing process can degrade the accuracy of read operations.

**2.3. Voltage and Current Sense Amplifiers in SRAM**

**T. Meenu Rani Garg, "A Study of Different Types of Voltage & Current Sense Amplifiers used in SRAM," International Journal of Advanced Research in Computer and Communication Engineering, p. 6, Vol. 4, Issue 5, May 2015.**

While voltage and current sense amplifiers are essential components in SRAM arrays for reliable read and write operations, they are subject to certain limitations that affect their performance and efficiency. One of the primary limitations is related to the trade-off between speed and power consumption. Voltage and current sense amplifiers must operate quickly to minimize access times in SRAM arrays, but this often comes at the expense of increased power consumption. Traditional sense amplifier designs may exhibit high static power dissipation due to leakage currents in the active devices or dynamic power dissipation during switching transitions. Finding innovative approaches to reduce power consumption without compromising speed is a key challenge in sense amplifier design for SRAM applications.

Another limitation lies in the sensitivity and robustness of sense amplifiers to noise and variations in operating conditions. In high-speed SRAM arrays, signal integrity is crucial, and any noise introduced during sensing or amplification can degrade the accuracy of read operations. Moreover, variations in process parameters, temperature, and supply voltage can affect the performance and reliability of sense amplifiers, leading to inconsistencies in operation and potential failures.

**2.4. Comparative Analysis of Sense Amplifiers**

**K. V. A.Hemprabha, "Comparative analysis of sense amplifiers for memories," IEEE, p. 6, 2015.**

The comparative analysis of sense amplifiers for memories involves examining various design aspects and performance metrics to evaluate their effectiveness and limitations. One significant limitation in the comparative analysis of sense amplifiers is the trade-off between speed and power consumption. Faster sense amplifiers may consume more power due to increased switching activity and higher operating frequencies. Conversely, low-power designs may sacrifice speed, leading to longer access times and reduced overall performance.

Another limitation is the susceptibility of sense amplifiers to noise and interference. As memory technologies advance and densities increase, the signal-to-noise ratio becomes a concern, impacting the accuracy and reliability of read operations. Noise sources such as process variations, temperature fluctuations, and electromagnetic interference can introduce errors or degrade the quality of sensed signals, affecting the overall performance of the memory system.

Moreover, the scalability of sense amplifiers poses challenges in adapting to evolving memory technologies. As memory densities continue to grow and feature sizes shrink, sense amplifier designs must accommodate smaller node sizes and tighter constraints, such as reduced power supply voltages and increased parasitic capacitances.

Additionally, the complexity and area overhead associated with advanced sense amplifier designs are limiting factors. More sophisticated sensing techniques and circuit topologies may improve performance but require additional circuitry and resources, leading to increased chip area and manufacturing costs.

**CHAPTER 3**

**EXISTING METHOD**

**3.1. TECHNIQUE FOR OPEN BIT ARCHITECTURE OF DRAM SENSE AMPLIFIER**

In this proposed technique, we are utilising the DRAM sense amplifier along with the FSPA-VLSA (Foot Switch PMOS Access Voltage Latch Type Sense Amplifier). The DRAM memory array is divided into the two halves, where FSPA-VLSA is placed in the middle of the circuit [9]. This is clearly illustrated in Fig 2, where it consists of two cross coupled inverters. The same input “SENSE” is applied to the PM2, PM3 and NM2. Bit lines BLL (Bit line left) and BLR (Bit line right) is connected with the output of the FSPAVLSA. On each side of the circuits, a column of dummy cell is added whose sole purpose is to serve as references. Here, NM5 and NM8 along with their storage capacitances “Cs” is used as dummy cells which are shown in the shadow area of the circuits. Two DRAM cells each consist of one NMOS and one capacitor is presented at the left and right of the FSPA VLSA which is used for storing the data [10] in open bit architecture of dram sense amplifier.

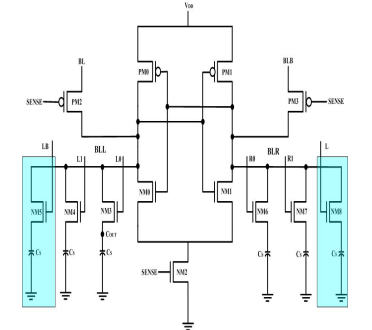


Fig.1: **Diagram technique for Open bit architecture of DRAM sense amplifier**

Firstly, we enable the L and LB lines at the same time to confirm that the dummy cells are charged with the voltage of VDD/2. Then, During the Read cycle one of the word line is enables from L0, L1, R0 and R1. So, we raise the Word line L0 as it is present in BLL which causes a voltage change in the BLL. Appropriate voltage is generated simultaneously by selecting the other dummy cell in other memory halves by raising L. Under this assumption, the BLL and BLR are perfectly matched resulting the BLR voltages reside in between the ‘0’ to ‘1’ value causes sense the latch to toggle.

**3.2. DISADVANTAGES**

**3.2.1 Power Savings:** One of the significant advantages of using 45nm technology in the design of DRAM sense amplifiers is the reduction in overall power consumption. By employing a Foot Switch PMOS Access Voltage Latch Type Sense Amplifier (FSPA-VLSA) in the open bit architecture of DRAM cells during read operations, the power savings are substantial. This technique allows for more efficient use of power, which is crucial for the development of energy-efficient memory systems.

**3.2.2. Advanced CMOS Technology:** The use of 45nm technology enables the integration of more complex and efficient circuits within the sense amplifier design. This technology allows for the implementation of advanced features such as latch type sense amplifiers, which have been shown to reduce sensing delay and improve the overall performance of DRAM systems. The application of 45nm CMOS technology in the design of sense amplifiers not only enhances their functionality but also contributes to the reduction of on-chip area, further optimizing the design for power efficiency and performance.

**3.2.3. Improved Performance:** The integration of 45nm technology in DRAM sense amplifiers leads to improved performance parameters. This includes reduced sensing delays, which are critical for the fast data access required by modern computing systems. The use of advanced CMOS technology in the design of sense amplifiers allows for the optimization of these parameters, ensuring that the DRAM system operates at high speeds while maintaining low power consumption.

**3.2.4. Reduced Soft Error Rate (SER):** The design of DRAM sense amplifiers using 45nm technology also contribues to the reduction of the soft error rate (SER). By employing advanced structures and concepts such as new dummy cell concepts, the SER of DRAMs can be significantly reduced. This is crucial for ensuring the reliability and integrity of data stored in DRAM systems.

**CHAPTER 4**

**PROPOSED METHOD**

**4.1. Power Gating**

In this chapter, the modification in the proposed circuit for DRAM in this design we are going to add the power gating technique to the PMOS. Here, the PMOS is designed using POWER GATING Logic. Here, we also mention the detailed information relating to power gating technique and the advantages towards the modified design.

**Introduction to Power Gating Technique:**

Power gating is a technique used in integrated circuits to reduce power consumption by turning off the power supply to specific circuit blocks when they are not needed. This technique is particularly useful in modern chips, which often contain many different functional blocks that may not be used at all times.

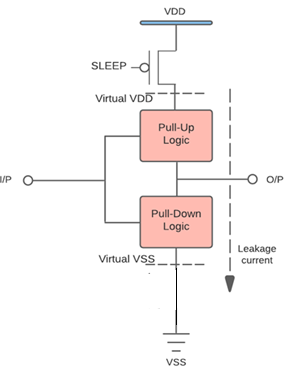


Fig. 2: Block diagram of Power gating technique

Power gating works by inserting switches into the power supply paths of specific circuit blocks, which can be controlled by a power management unit. When the circuit block is not needed, the switch is turned off, cutting off the power supply and reducing the power consumption of the circuit.

Power gating is typically used in conjunction with other power management techniques, such as dynamic voltage and frequency scaling (DVFS), to further reduce power consumption in integrated circuits. However, power gating can also introduce some design challenges, such as increased complexity and potential timing issues when switching between power states.

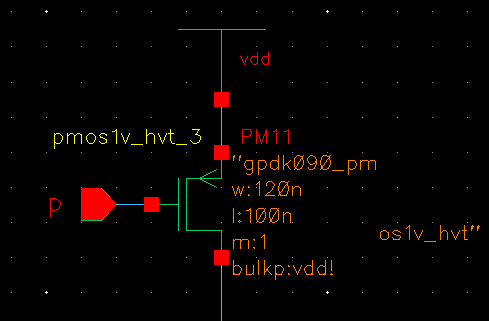
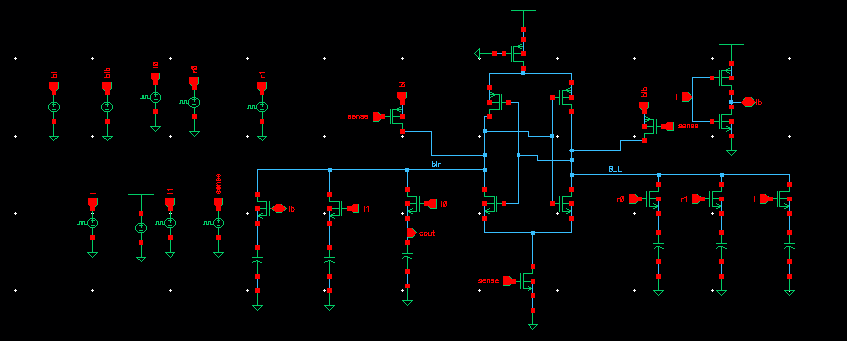


Fig. 3: PMOS Transistor for Power Gating Technique

Despite these challenges, power gating is an effective technique for reducing power consumption in integrated circuits and is widely used in many modern electronic devices, such as smartphones, laptops, and other portable electronics.

This is the diagram of the power gating technique we applied in this diagram in previously the vdd supply we are going to applied directly & now coming to extension part we are applying power gating to pmos transistor & vdd supply via that pmos transistor, after adding this technique our design power consumption is going to be reduced .

Fig. 4: The proposed circuit diagram with power gating technique

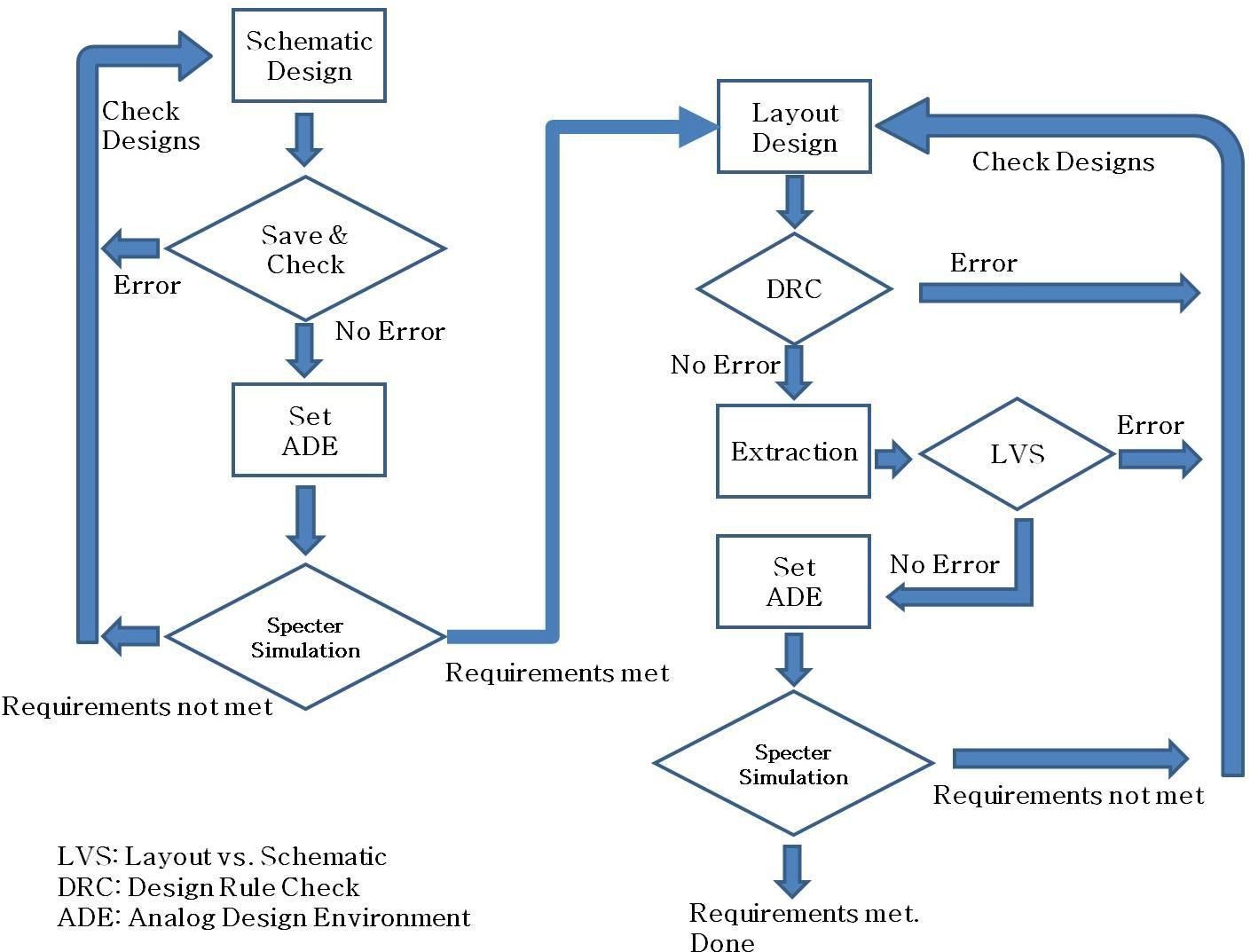
The proposed circuit diagram is shown in the above figure as we applied low power technique that is power gating logic & the load resistor at the output side we are going to increase the value of that resistor because of increasing the value gain, compare to exciting method our gain is going to be improved.

The schematic shown represents a **6-transistor (6T) SRAM memory cell array with peripheral circuitry** designed in a CMOS technology. At the center is the SRAM cell, consisting of **two cross-coupled inverters** and **two access transistors** connecting the cell to the bitlines (BL and BLR). The bitlines interface with **sense amplifiers** and **write drivers** for read and write operations. Wordlines control the gates of the access transistors to enable or disable connections to the bitlines during read/write cycles.

On the left side are multiple **input control signals** (I0–I7), connected via inverters and pass transistors, likely functioning as part of decoder or precharge logic. On the right are similar circuits connected to **output or sense amplifier controls**. The sense amplifier amplifies the small voltage difference between BL and BLR during read operations. This schematic represents the **circuit-level design of a memory block**, combining storage, read/write access, and sense amplification for reliable operation in digital systems.

**CHAPTER 5**

**TOOL CONTENT**

**5.1 OVERALL DESIGN FLOW**

**FIG 5: Analog IC Design Flowchart from Schematic to Layout Verification**

The process of creating a new library in Cadence Virtuoso and attaching it to a technology library is fundamental for any analog or digital IC design project. The provided images clearly illustrate each step involved. First, as shown in the initial image, you begin by opening the Library Manager and navigating to File → New → Library. This action opens a dialog box where you can specify the name of your new library (as seen in the second image). Here, you enter a meaningful name, such as "demo," and select the directory where the library will be stored. This organization is crucial for keeping your design files structured and accessible.

After naming your library, you are prompted to attach a technology file. The fourth image shows the "Technology File for New Library" dialog, where you select Attach to an existing technology library. This step ensures that your new library inherits all the necessary process design rules, device models, and parameters from the foundry-specific technology library, which is essential for accurate design and simulation. Clicking OK brings up the third image, where you select the specific technology library (for example, NCSU\_TechLib\_tsmc02) that matches your intended process node.

Once you confirm your selection, the new library appears in the Library Manager, fully configured and ready for use. This setup allows you to proceed confidently with schematic entry, simulation, layout, and verification, knowing your designs are compliant with the chosen technology. This step-by-step process is a critical foundation for successful IC design in Cadence.

**1. Open Library Manager (Image 1):**

* Launch Cadence Virtuoso.
* Go to **File → New → Library** in the Library Manager window.

**2. Name Your Library (Image 2):**

* In the "New Library" dialog, enter your desired library name (e.g., "demo").
* Choose the directory where your library will be stored.
* Click **OK** to proceed.

**3. Attach Technology File (Image 4):**

* In the "Technology File for New Library" window, select **Attach to an existing technology library**.
* Click **OK** to continue.

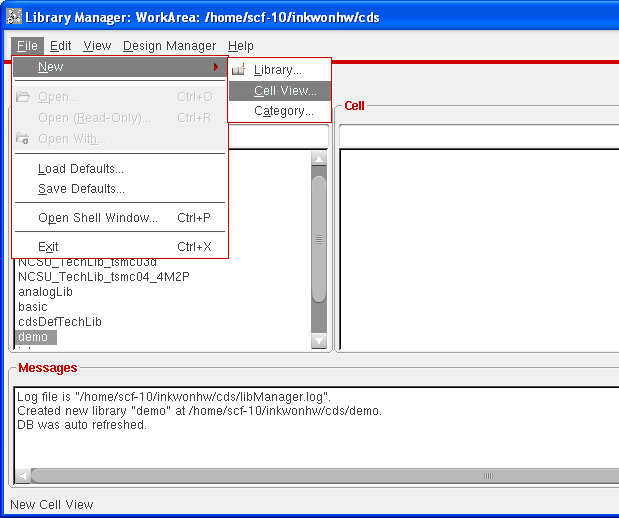
**4. Select Technology Library (Image 3):**

* In the "Attach Library to Technology Library" dialog, select the appropriate technology library (e.g., NCSU\_TechLib\_tsmc02).
* Click **OK** to finish the process.

**5. Library Ready:**

* Your new library is now created, attached to the correct technology, and ready for design work.
  1. **SCHEMATIC**

1. **Create a cell view**

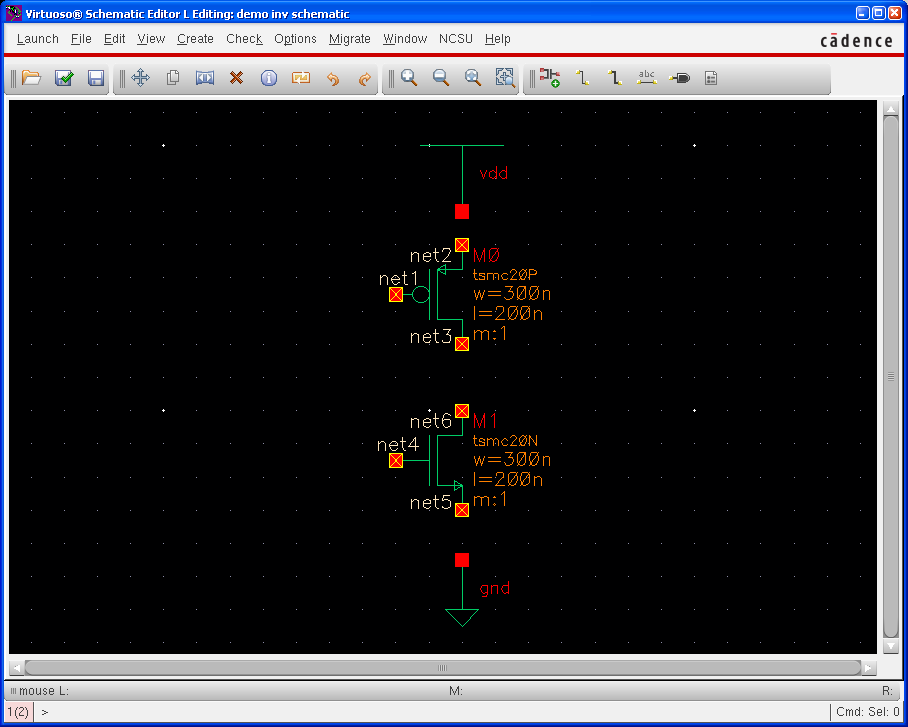
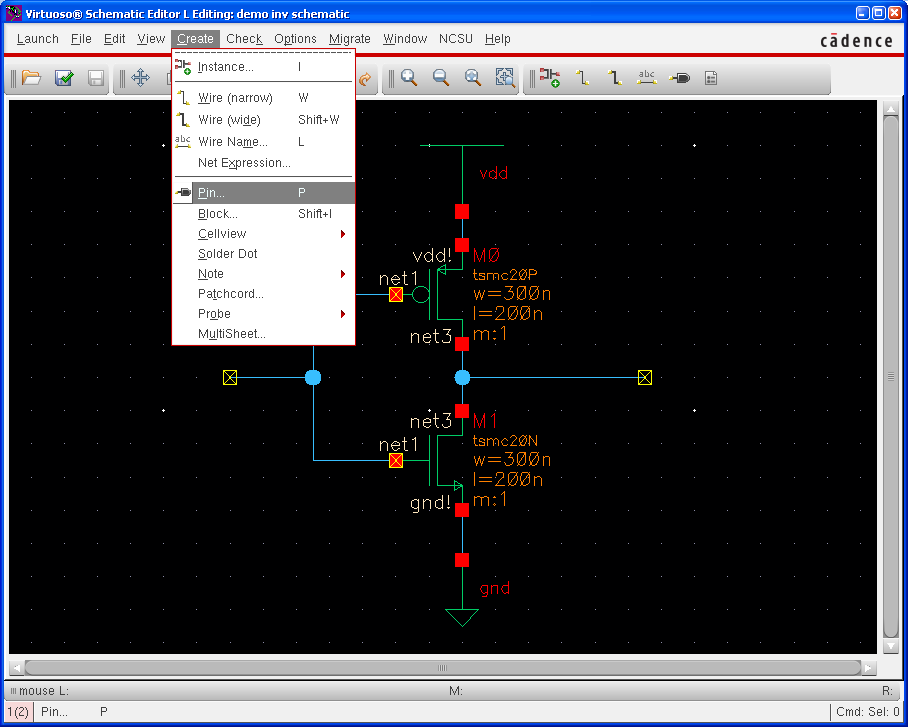
 Select the library just created, File->new

**Fig 6 : File creation in cadence to create new cell**

**Draw a schematic**

1. Add instances – pmos you can modify Width of transistors. Don’t modify length unless you have a special purpose. You should select an NCSU\_Analog\_Parts library
2. **M0 (PMOS transistor)**: Connected to VDD (power supply)
3. **M1 (NMOS transistor)**: Connected to GND (ground).
4. **Input (in)**: Applied to the gates of both transistors.
5. **Output (out)**: Taken from the connection between the PMOS and NMOS transistors.

This is a fundamental building block in digital logic design, used to invert the input signal.

 **Fig 7: instances – nmos, vdd, and gnd**

**Fig 8 : Schematic of CMOS inverter circuit**

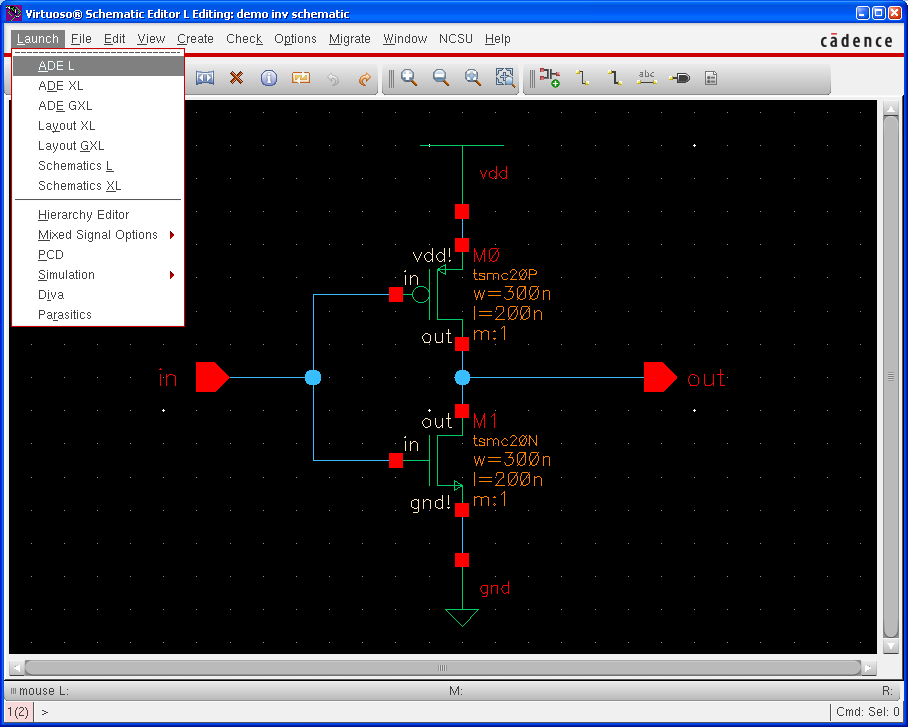
This schematic, created in Cadence Virtuoso Schematic Editor, represents a CMOS inverter-a fundamental digital logic gate. The circuit consists of a PMOS transistor (M0) at the top, connected to the supply voltage (vdd), and an NMOS transistor (M1) at the bottom, connected to ground (gnd). Both transistor gates are tied together and form the input node ("in"), while their drains are connected to the output node ("out"). When the input is high, the NMOS conducts and the PMOS turns off, pulling the output low. Conversely, when the input is low, the PMOS conducts and the NMOS turns off, pulling the output high. This configuration ensures the output is always the logical inverse of the input. The schematic also shows transistor sizing (w = 300n, l = 200n, m = 1), which influences the inverter's performance.

We have for different types of direction. For schematics, we only use two types, input and output. Input/output type is for supply changes, and it is necessary only for layout. We will discuss about this later.

Check and save  to make sure there are no errors. Now, we completed a schematic design.

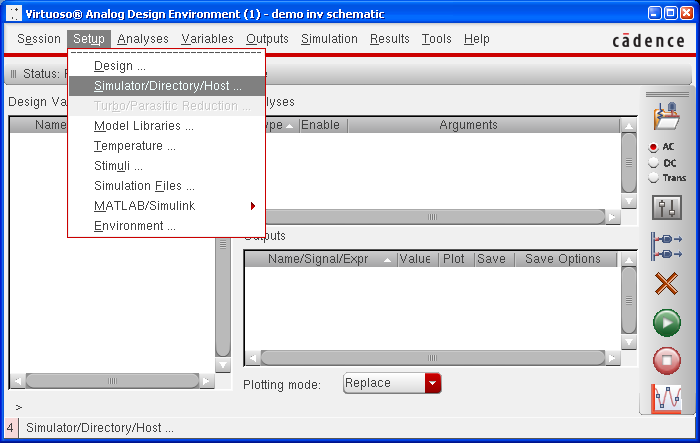
Remember that when you use more than one symbol in schematic, they all will have common Vdd and Gnd even if there are one Gnd and Vdd for each symbol (in the original design). To design with symbols in layout, you should make sure that all of the Vdd and Gnds are connected.

* 1. **Run Spectre simulation (Transient analysis)**

We will run spectre simulation. This section is for **both** schematics and layouts. I will show an example for a schematic. You can do the same thing for a layout.

**Fig 9 : Launch ADE (Analog Design Environment)**

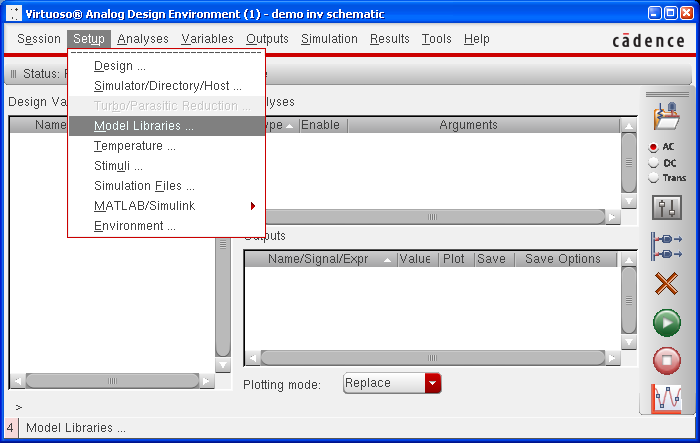
1. **Basic setup**

Check if your simulator is spectre. You can modify project directory.

**Fig 10 : Layout of simulator in cadence**

1. **Model Libraries**

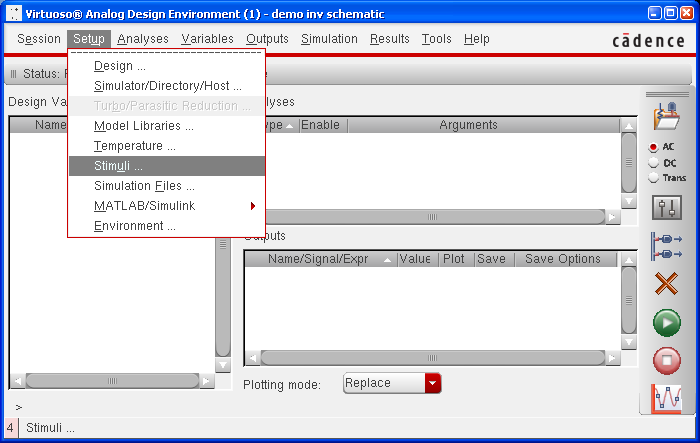
You can download a library file at the DEN blackboard.

Put the tech file under /home/scf-10/your-user-name/cds/techfiles/

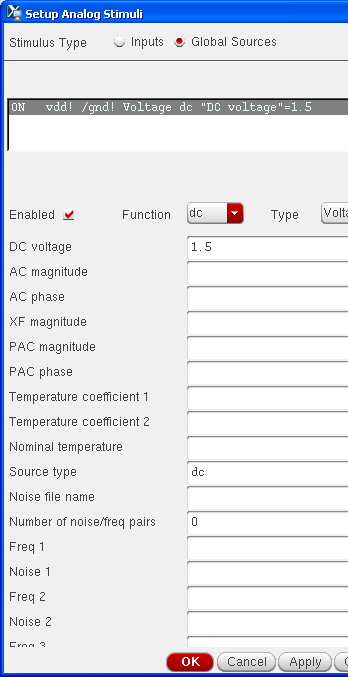
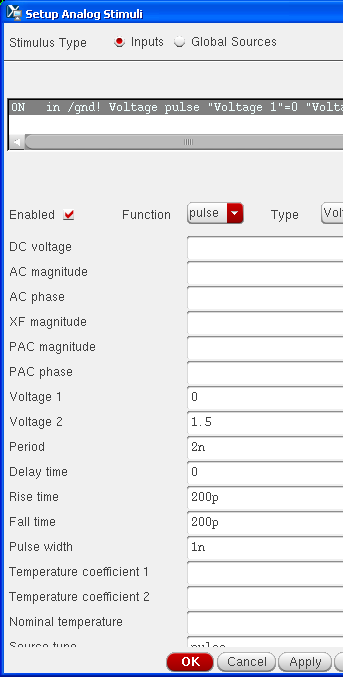
**Fig 11 :Model Libraries in Cadence**

Please only use the provided tsmc file because some tsmc files does not work correctly.

1. **Stimuli**

Define input signals include supply nets (for layout, vdd! and gnd! are under inputs and both should be enabled.)

**Fig 12 : Supply nets in Cadence-Stimuli**

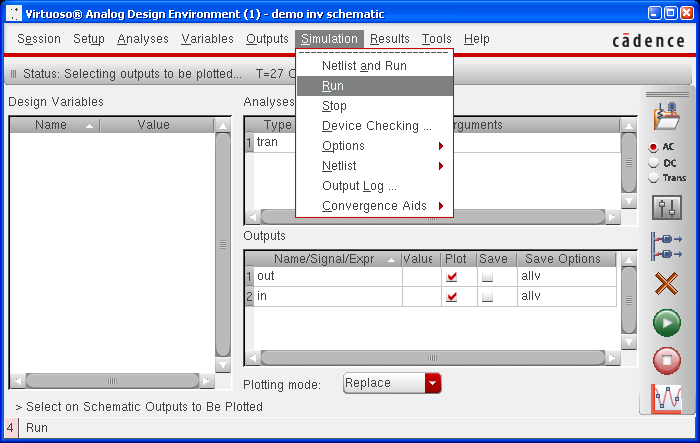
Global sources Input (change)

**Fig 13 :Global sources in Cadence Fig 14 :Input for the Schematic**

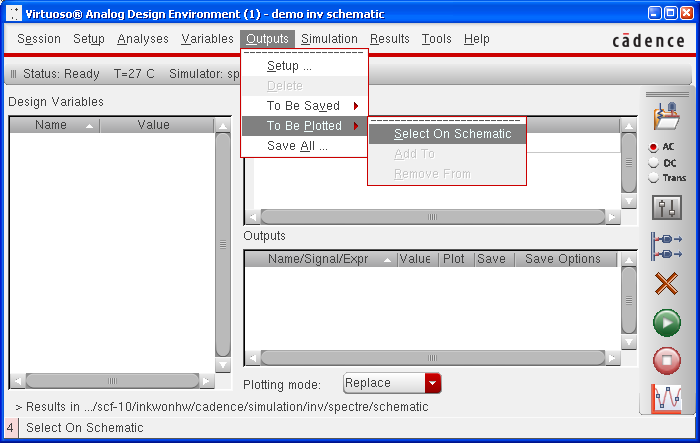
Remember to check Enabled button and then press OK or APPLY otherwise you will lose the configured numbers.

1. **Choose a type of analysis – transient**
2. Choose Tran
3. Give Stop time which means how long you want to

simulate

1. Select moderate as accuracy defaults
2. Do not check Transient Noise
3. Check Enabled
4. **Select signals to plot**

**Fig 15 :Simulation of the Schematic**

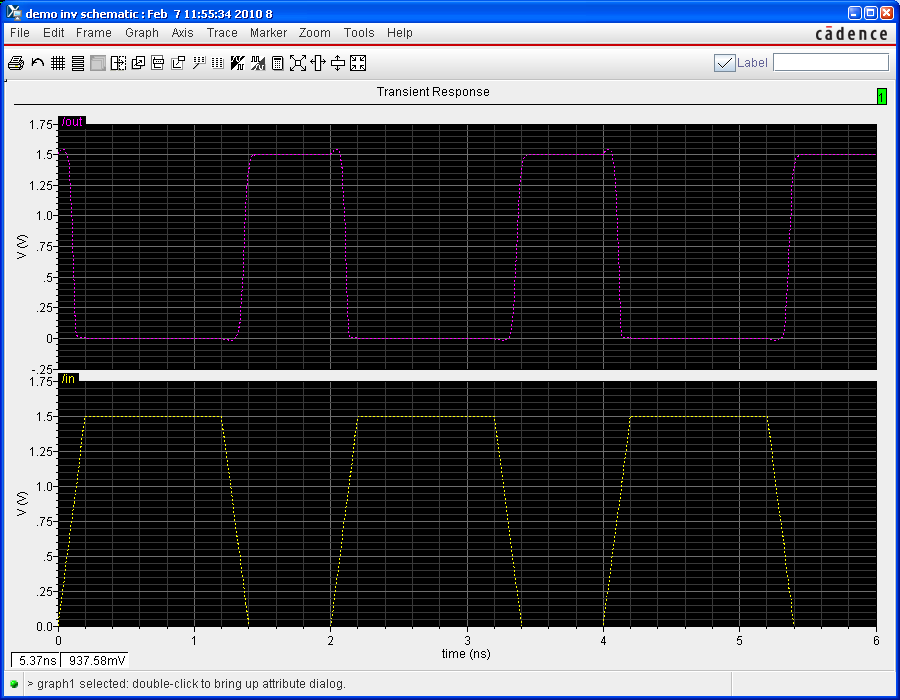
Outputs  to Be Plotted  Select On Schematic

**Fig 16:Input Signals to be plotted**

Click a signal (Pin) on a schematic/extracted. In Extracted try to use pins for signal that you need in the simulation because it is hard to select a net in the extracted view.

1. **Run simulation**

Simulation  Run



**Fig 17 :Waveform of Transient Analysis**

If you see a waveform like above picture, you followed every step properly.

The waveform displayed shows the **transient response** of a CMOS inverter simulated in Cadence. The plot includes two signals: **input (V\_in)** in yellow at the bottom and **output (V\_out)** in purple at the top, both plotted against time in nanoseconds (ns). As expected from an inverter, the output signal is the **logical inverse** of the input.

When the input voltage transitions from high (~1.7 V) to low (0 V), the output correspondingly switches from low to high, and vice versa. The sharp transitions in the output demonstrate good switching behavior, indicating that the inverter is functioning correctly with minimal delay and distortion. The simulation verifies the inverter’s transient performance, showcasing propagation delay and signal integrity across switching events. This type of analysis is crucial for evaluating timing characteristics and ensuring reliable digital logic operation in integrated circuits.

1. **Measurement**

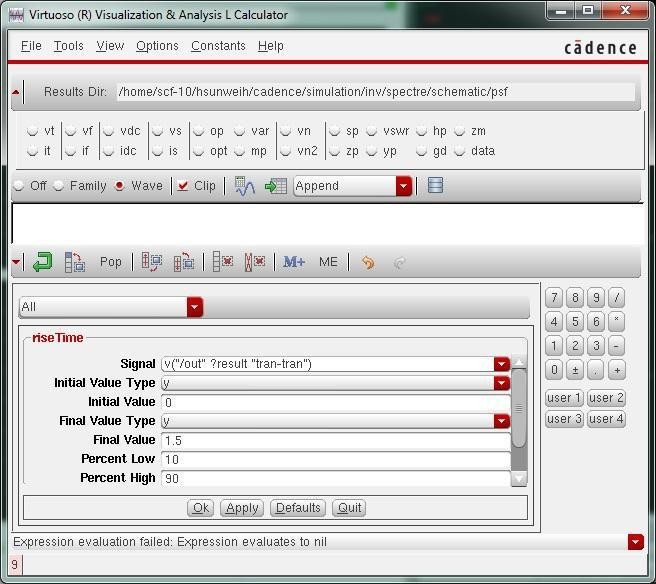
The following steps describe the measurement of rise time. Using similar steps other parameters of delay, fall time can be estimated.

Invoke the calculator  or tools-> calculator, select the Wave radio button:

In the functions window – choose “all”

Select the rise time option

Select the signal from the waveform window whose rise time needs to be determined and click “OK”:

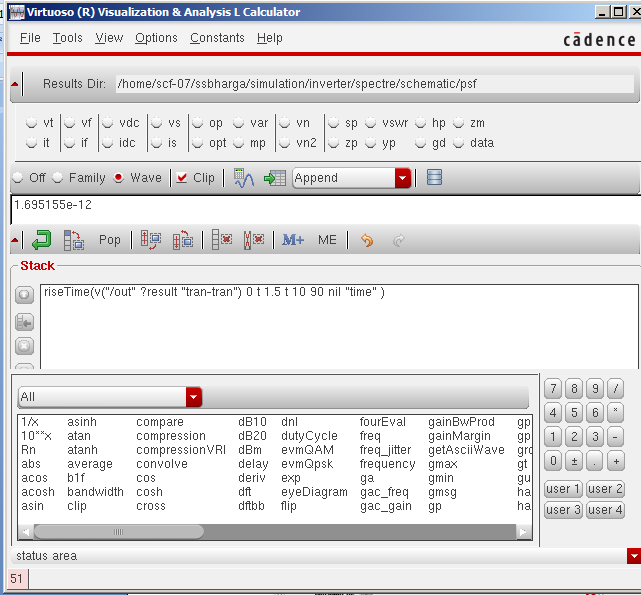


**Fig 18 : Calculation of rise time**

Click the evaluate buffer  to display results as follows

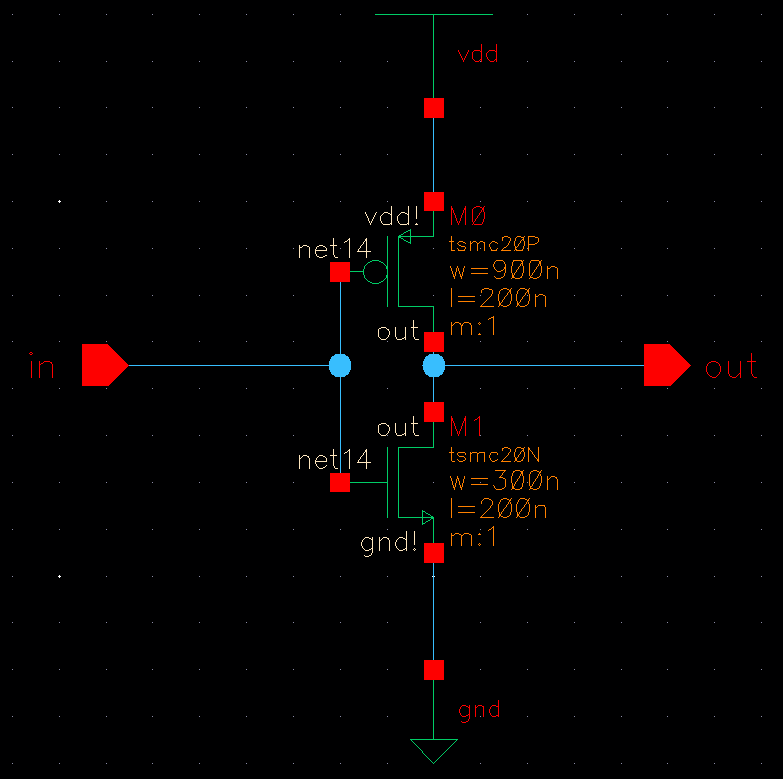
You can also select a signal from calculator for example cos (Vin) as one of the plotted signals and you can see the results whenever you run the simulation.

Remember to save the simulation setup to use it later. You can do so by clicking on **Session**  **Save State** in the ADE (Analog Design Environment) window. Next time you want to simulate the same cell, you can reload your configuration by clicking on **Session**  **Load State**.



**Fig 19 : rise time at transient analysis**

**5.4 Run Spectre simulation (DC analysis)**

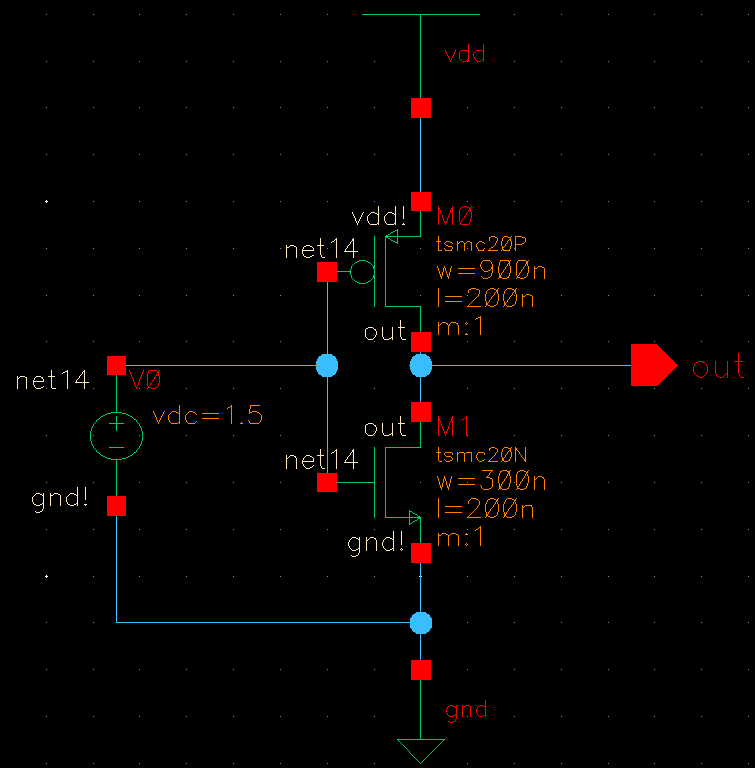
The following inverter schematic is already created

**Fig 20 : CMOS inverter circuit schematic**

For DC analysis, the input pin “in” must be altered. The following are the steps to alter the pin “in”: CreateinstanceNCSU analog partsVoltage\_sources select Vdc. The DC voltage must be set to 1.5V as shown.

This schematic represents a CMOS inverter circuit designed using TSMC 20nm technology. It consists of two transistors: a PMOS transistor (M0) connected to VDD at the top and an NMOS transistor (M1) connected to GND at the bottom. The input signal is applied to the gates of both transistors, while the output is taken from the node where the drains of both transistors are connected. The PMOS transistor has a width of 900 nm and a length of 200 nm, while the NMOS transistor has a width of 300 nm and a length of 200 nm, indicating a sizing ratio of 3:1 to balance the drive strength. When the input is high, the NMOS turns on and pulls the output low; when the input is low, the PMOS turns on and pulls the output high. This configuration provides the basic inverter function with rail-to-rail output swing and is a fundamental building block in digital logic design.

1. **Replace Input Pin**

The Input pin “in” must be replaced with the above voltage source as shown below

**Fig 21:**  **CMOS inverter circuit schematic with Voltage source**

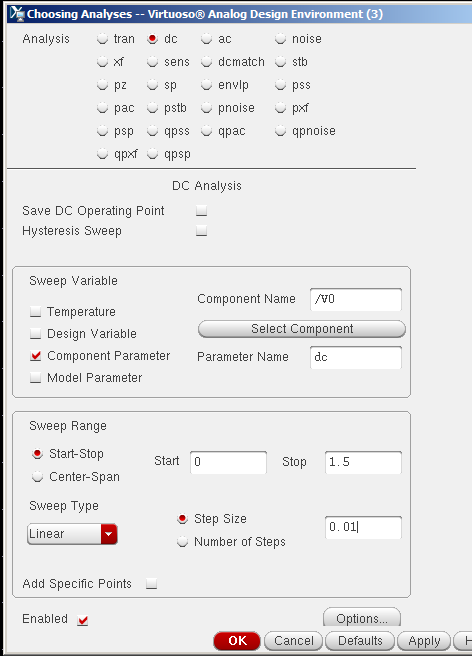
The schematic represents a CMOS inverter circuit with a DC voltage source (V0) applied at the input node for DC analysis. The inverter consists of a PMOS transistor (M0) and an NMOS transistor (M1) fabricated using TSMC 20nm technology. The PMOS has a width of 900 nm and a length of 200 nm, while the NMOS has a width of 300 nm and the same length of 200 nm, providing a width ratio of 3:1 to balance their drive strengths.

The voltage source V0 = 1.5 V is applied at the input node, allowing analysis of the inverter's DC transfer characteristics at this specific input voltage. The output node is connected at the drains of both transistors, which will be pulled either to VDD or GND depending on the input voltage level. This configuration is commonly used for DC sweep simulations to generate the voltage transfer curve (VTC), critical for determining the inverter’s threshold voltage, noise margins, and switching behavior.

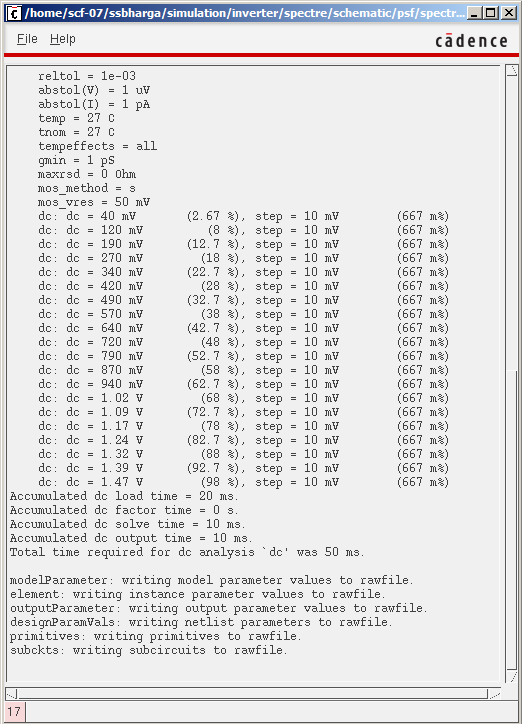
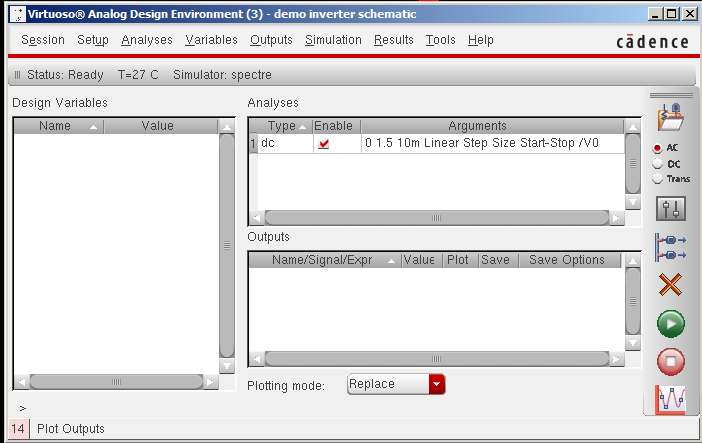
1. **Choosing Analyses**

Launch ADE L, repeat steps A to D in section 3 of „Basic Design Flow‟ except that there is no “in” input signal this time.Go to Analyses  Choose dc Choose „Component Parameter‟,.

0.01 as step .



**Fig 22 : DC Analysis Setup in Virtuoso ADE**

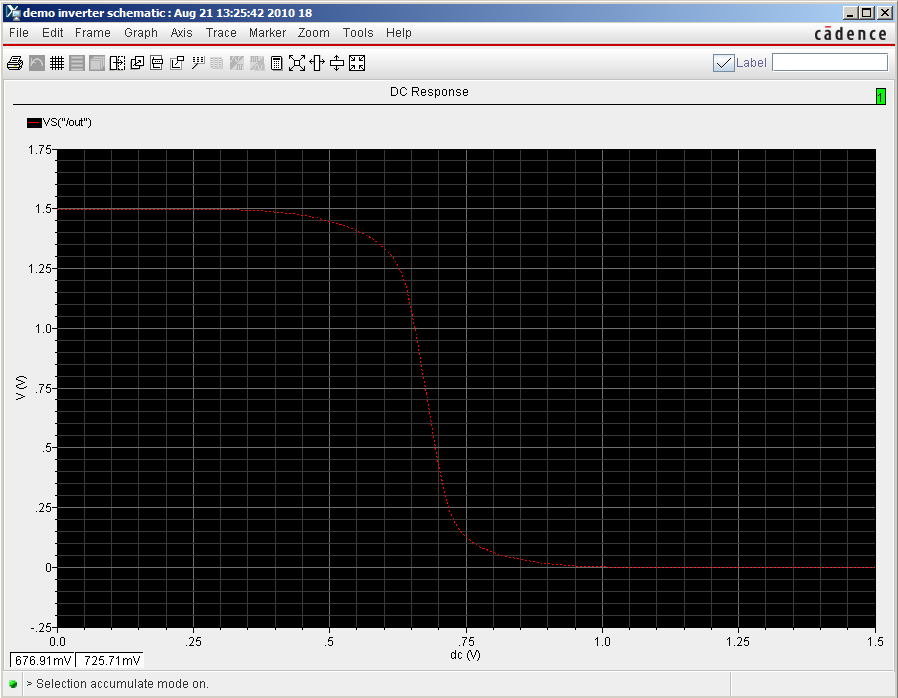


**Fig 23 : DC Sweep Simulation Log in Cadence Spectre**

Simulation setup and execution results for a CMOS inverter using the Cadence Virtuoso Analog Design Environment with Spectre as the simulator. The first image displays the Spectre simulation log for a DC sweep analysis, where the input voltage is swept from 0 V to 1.5 V in 10 mV steps. The log confirms successful completion of the DC analysis, indicating convergence at each step and reporting simulation times. The second image shows the Analog Design Environment setup, where a DC analysis is configured with a linear sweep from 0 V to 1.5 V, a 10 mV step size, and no initial outputs plotted yet. This setup enables users to plot the inverter’s voltage transfer characteristics (VTC) by observing the relationship between input and output voltages. The simulation provides valuable insights into the switching threshold and noise margins, essential for verifying inverter performance in digital integrated circui

**Run Simulation**

Do simulationsnetlist and run. On successful completion we get the following

Now, go to the resultsDirect plotDC. Click on the output pin “out” on the schematic and ESC key to get the following VTC

**Fig 24: Simulation of CMOS inverter in DC analysis**

The image displays the DC transfer characteristic of a CMOS inverter, simulated using Cadence. The X-axis represents the input voltage (V\_in) swept from 0 to 1.5 V, while the Y-axis shows the output voltage (V\_out) ranging from 0 to approximately 1.7 V. Initially, when the input is low (close to 0 V), the output remains high (near the supply voltage), demonstrating the inverter’s logic. As the input voltage increases and approaches the threshold region (around 0.7 V), the output voltage rapidly drops, marking the inverter’s switching point. Beyond this threshold, as the input continues to rise, the output voltage settles near 0 V, confirming the inverter action. The sharp transition in the curve indicates strong gain and good noise margins, essential for digital circuit reliability. This characteristic is fundamental for verifying the correct operation and sizing of CMOS inverters in digital design.

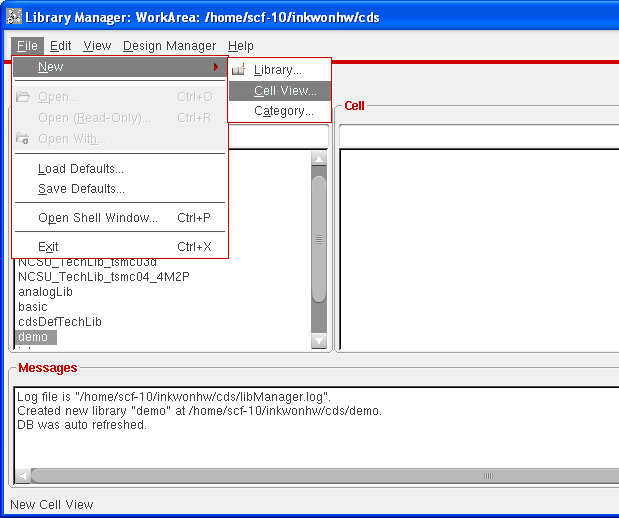
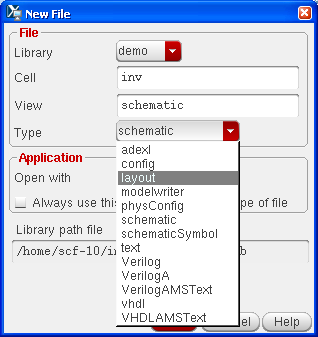
**CHAPTER – 6**

**LAYOUT DESIGNING**

**6.1 LAYOUT**

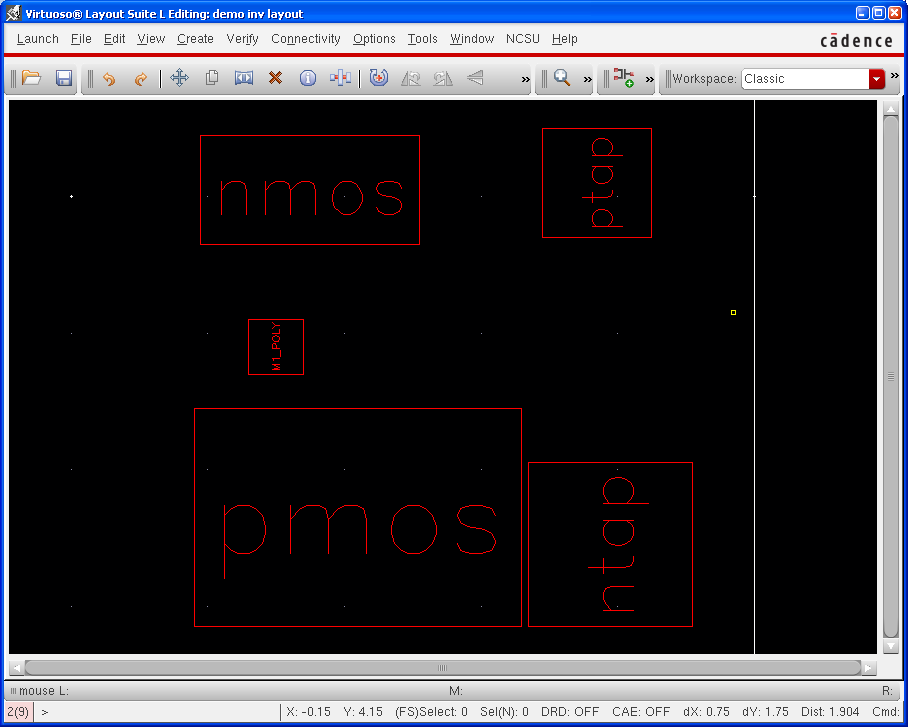
It’s time to draw layout. Schematics are for verifying your design very roughly. They don‟t consider physical features like parasitic capacitances. After determining your design variables by schematics, you need to draw layouts.

Design flow of layouts is very similar to one of schematics, but it has additional step which is LVS check. It is for check if your layout is identical to the schematic or not. Hence, this step is very important. If your logic doesn‟t pass this step, you may lose significant points for that.

* 1. **Create a layout**

**Fig 25 : Creating a New Cell View in Cadence Virtuoso**

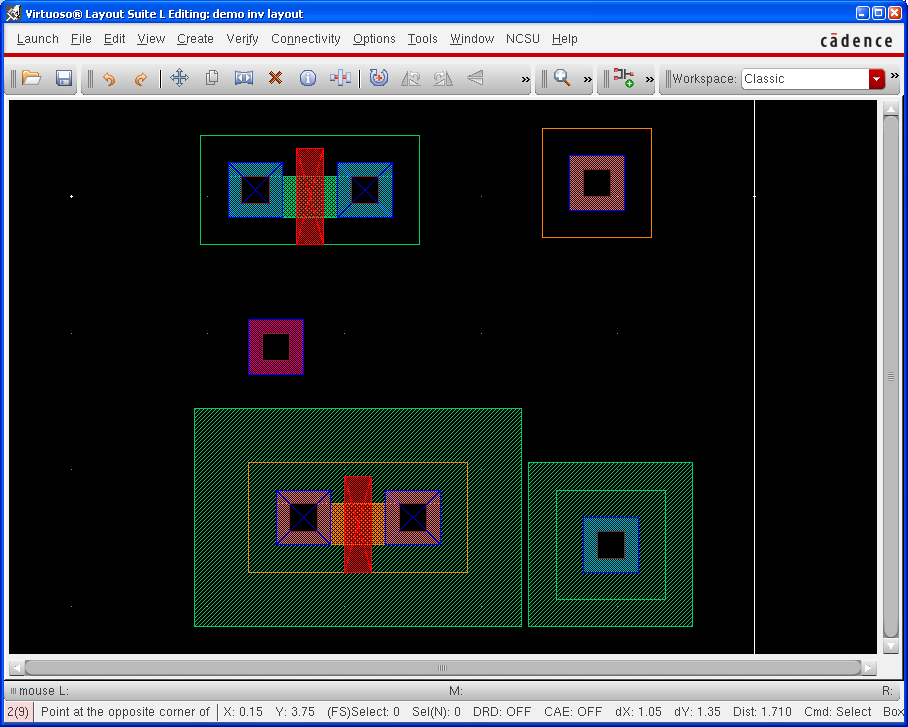
The user is accessing the File → New → Cell View option to create a new schematic, symbol, or layout view.It allows hierarchical design organization by linking Library, Cell, and View levels.The Library groups related designs, Cell is a circuit or block, and View can be schematic, layout, symbol, etc.  he bottom pane shows the message log, indicating successful creation of the library “demo.” This step is essential before designing circuits like inverters, amplifiers, or memory cells.The platform used here includes the NCSU\_TechLib\_tsmc03 and cdsDefTechLib process libraries.

**Add more instances – pmos, pta ntap, and m1\_ploy**

**Fig 26 : Instances – pmos, pta ntap, and m1\_ploy**

Image shows the layout design of a CMOS inverter in Cadence Virtuoso Layout Suite, where key components are visually represented by labeled blocks. The layout contains the PMOS and NMOS transistors, along with ntap and ptap regions for substrate contacts, which are essential for proper biasing and to avoid latch-up.

In this layout, the PMOS is positioned above the NMOS, reflecting a typical CMOS layout structure where PMOS resides in the n-well and NMOS in the p-substrate. The ntap (n+ diffusion tied to VDD) and ptap (p+ diffusion tied to GND) provide well and substrate contacts, respectively, to maintain stable potentials. This schematic-level abstraction aids in understanding the physical placement of devices prior to full polygon-level mask design. Such a layout is critical for ensuring design rule compliance, proper connectivity, and minimizing parasitic effects in integrated circuit fabrication.

You can select alternate view of a layout. Try „Shift + f‟ and „Ctrl + f‟.

**Fig 27 : Layer Representation of CMOS Inverter**

**Draw metal1**

There are few ways for drawing metal, but I recommend you use „path‟. It‟s quite convenience than others.

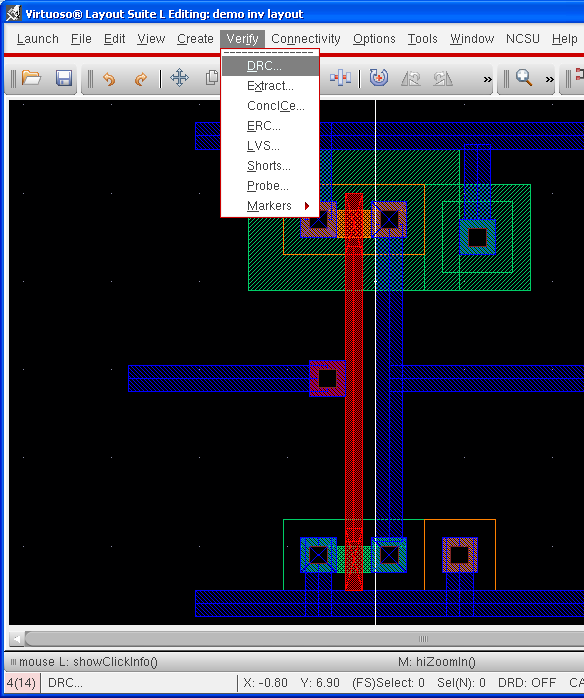
Create  Shape  Path

First of all, you should select metal1 on LSW window. Default width for metal1 is 0.3, which means 300nm (3 λ). You can draw metal layer simply by clicking

Image shows the **polygon-level layout view of a CMOS inverter** in **Cadence Virtuoso Layout Suite**. It represents the detailed physical design, with **different colored layers.** This layout would need DRC (Design Rule Check) and LVS (Layout vs Schematic) verification to ensure compliance with process rules and schematic functionality. It’s the final step before sending the design for mask generation and fabrication.

**Run DRC**

This step checks if your layout follows design rules. Verify  DRC



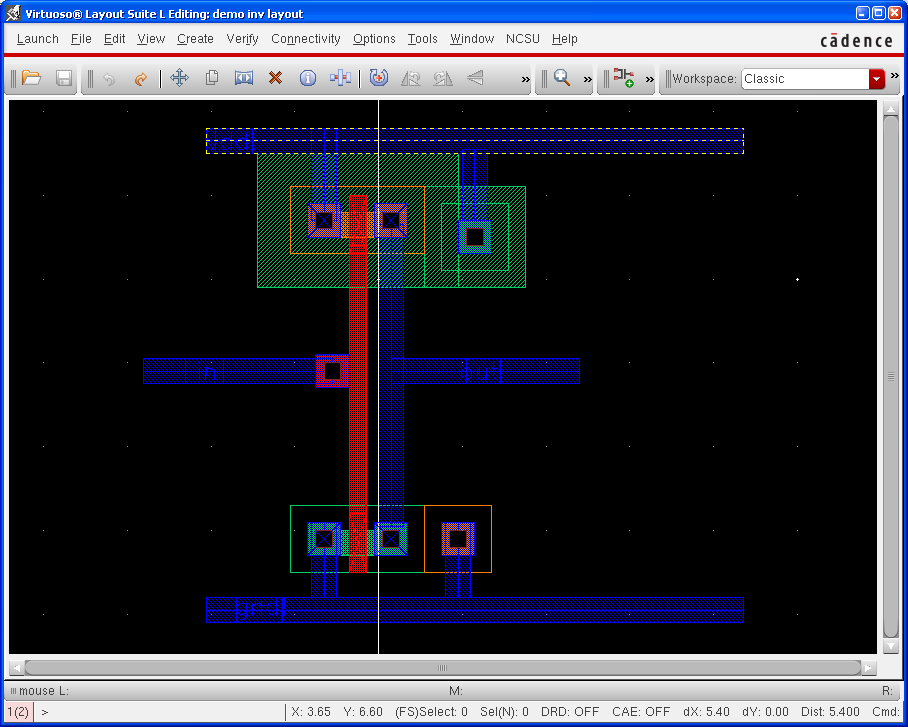
**Fig 28 :** **Highlighting Metal Connections and DRC Verification Menu**

**Add pins**

We had two pins on a schematic, which are „in‟ and „out‟. Pins are for assigning signals to physical device, so we assign voltage level of gnd and vdd by using pins. Hence, we have 4 pins for the layout, which are „in‟, „out‟, and „gnd! ‟, and „vdd! ‟.

Create  Pin

Check „Display Terminal Name‟ if you want to see pin name on the layout. Click „Display Terminal Option



**Fig 29 : Interconnections Using Metal Layers and Vias**

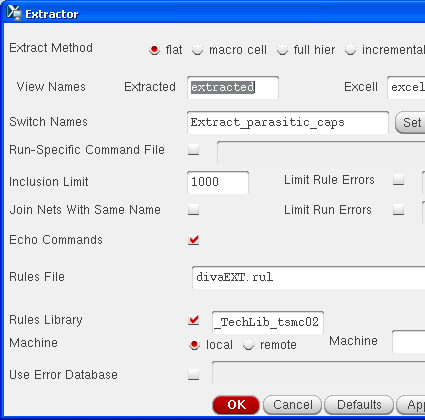
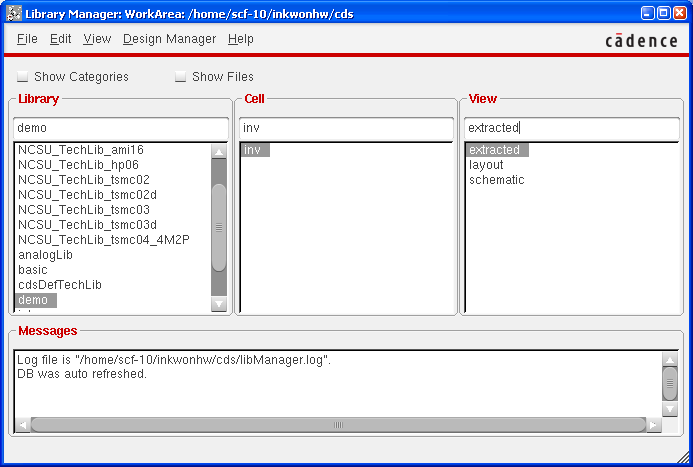
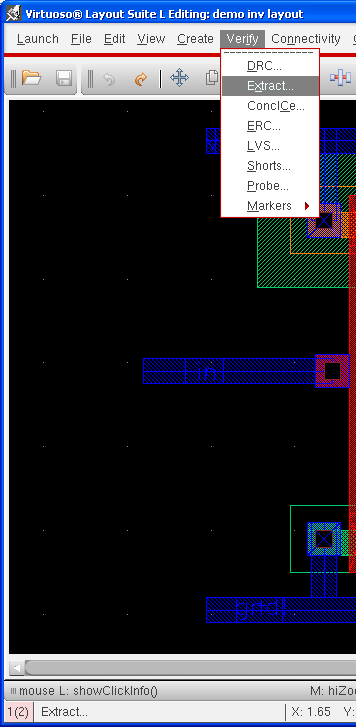
**6.2 LAYOUT EXTRACTION**

Verify the design using DRC to ensure no rule violations exist. Then, perform the extraction process to generate the netlist and parasitics from the layout. After extraction, check the extracted view and run an LVS check to confirm schematic and layout consistency. These steps help identify connectivity issues and validate the design before tape-out.

Steps to perform layout extraction:

1. Open the CMOS inverter layout from the Library Manager in Virtuoso.
2. Run DRC from *Verify > DRC* to check for rule violations.
3. Fix any DRC errors by editing the layout to meet design rules.
4. Go to Verify > Extract and enable extraction options.
5. View the extracted layout by opening the "extracted" cell view.
6. Run LVS from *Verify > LVS* to compare layout with schematic.
7. **Extract**

A layout is just a picture. If you need to run simulation using the layout, you should convert it to the other format. It is done by extracting. It’s something like compiling a code.



**Fig 30 : Extractor Settings and Extracted View in Library Manager**

Select „Extract\_parastic\_cap‟ as a switch name, otherwise your extracted design won’t have parasitic capacitances.

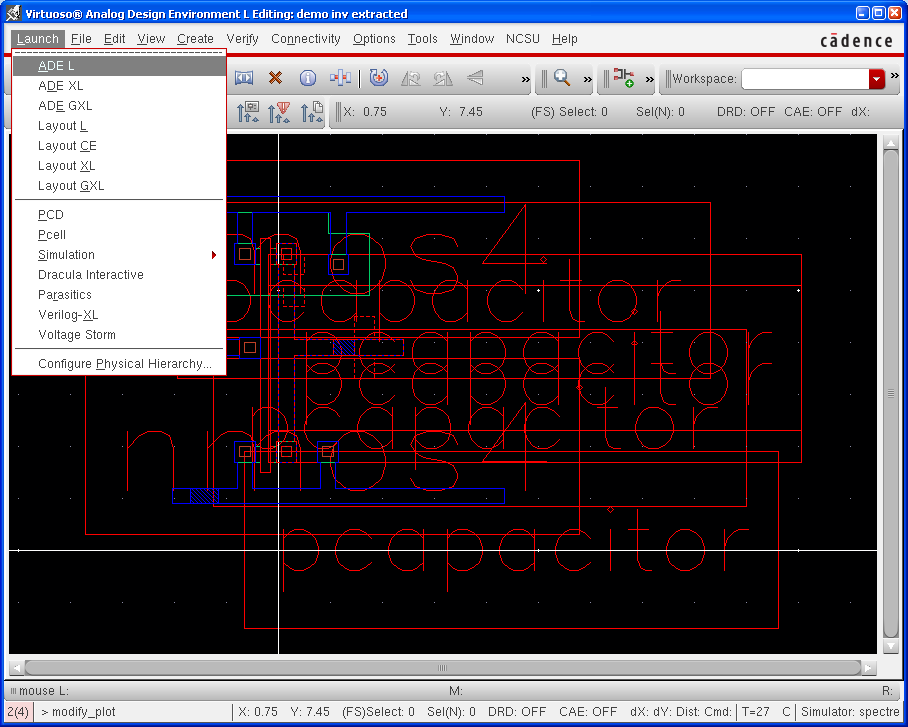
**Run LVS**

As I mentioned before, this step is very important for your grading. More complicated design, more time will be required for debugging LVS.

Verify  LVS

This image shows the process of **parasitic extraction in Cadence Virtuoso** for a CMOS inverter layout. The user selects **Verify → Extract** from the menu to launch the Extractor tool, configuring it to generate an **“extracted” view** using the technology rule file divaEXT.rul. This process analyzes the physical layout to extract parasitic capacitances and resistances introduced by interconnects and devices.

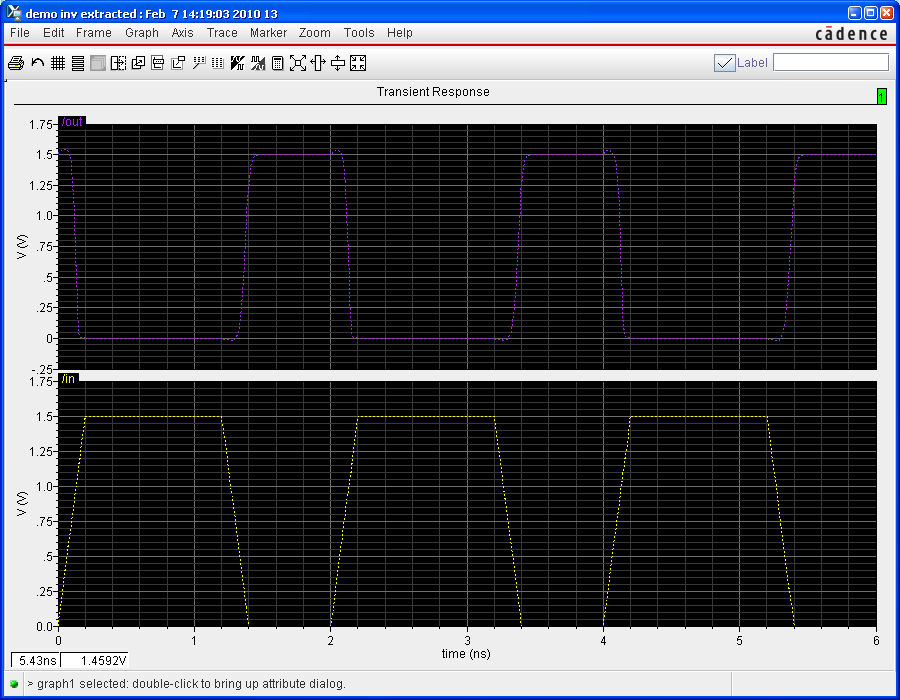
Once completed, the extracted view is visible in the Library Manager alongside the schematic and layout views, enabling further steps like **post-layout simulation or LVS (Layout vs. Schematic)** verification to ensure the layout matches the circuit design, considering real-world effects.

Keep in mind. You **SHOULD** compare your schematic with **EXTRACTED**.

**Fig 31:** **Visualization of Extracted View Showing Parasitic Components**

Extracted view of a CMOS inverter in Cadence Virtuoso showing parasitic components such as interconnect resistances and capacitances. These parasitics are automatically included during layout extraction using tools like Assura or PVS. The extracted netlist provides more accurate simulation results, allowing designers to evaluate real-world performance impacts, including delay, signal integrity, and power consumption. These parasitic elements are critical for post-layout simulation and timing analysis. Accurate modeling helps ensure the circuit meets performance and reliability requirements before fabrication.

1. **Run Spectre simulation**

It is same as schematics. Please follow the instructions for the schematics.

**Fig 32 :** **Transient Response of a CMOS Inverter.**

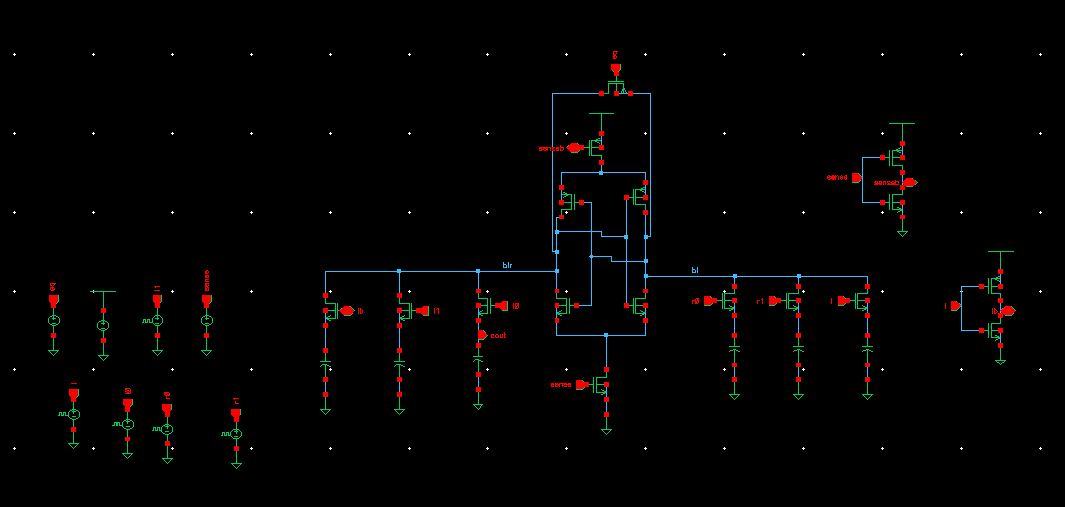
The graph in question represents the transient response of a CMOS inverter-specifically, how the output voltage (Vout*Vout*) responds over time to a changing input voltage (Vin*Vin*), considering the real-world effects of intrinsic capacitances within the circuit.

Key Aspects Illustrated by the Graph:

* Ideal vs. Actual Response:  
  Ideally, when the input voltage is low (Vin=0*Vin*=0), the output should instantly be high (Vout=VDD*Vout*=*VDD*), and when Vin*Vin* is high (Vin=VDD*Vin*=*VDD*), the output should instantly be low (Vout=0*Vout*=0). This would appear as a sharp, step-like transition in the output voltage as the input crosses the threshold.
* Effect of Capacitance:  
  In reality, due to the gate-to-drain capacitance (often labeled as Cgd*Cgd*) present in both the PMOS and NMOS transistors, the output does not change instantaneously. Instead, as the input voltage ramps up from 0 to VDD*VDD*, the output voltage initially follows the input for a brief moment due to capacitive coupling. This results in a momentary rise or dip in the output voltage before it transitions to its final value
* Transient Phenomena:
  + As Vin*Vin* increases and crosses the threshold voltage (Vtn*Vtn*) of the NMOS, the NMOS turns on, and the output is pulled down toward 0.
  + Before this point, due to the capacitive effect, the output may momentarily increase even as the input is rising, which is not observed in the ideal case.
  + Once the NMOS fully conducts, the output quickly falls to zero
* Propagation Delay:  
  The delay between the input crossing the threshold and the output responding is known as the propagation delay. This delay is a key parameter in digital circuits, as it limits the speed at which the inverter (and thus the entire circuit) can operate
* Rise and Fall Times:  
  The graph also demonstrates that the transition of the output is not instantaneous but occurs over a finite time, characterized by the rise time (output going from low to high) and fall time (output going from high to low)

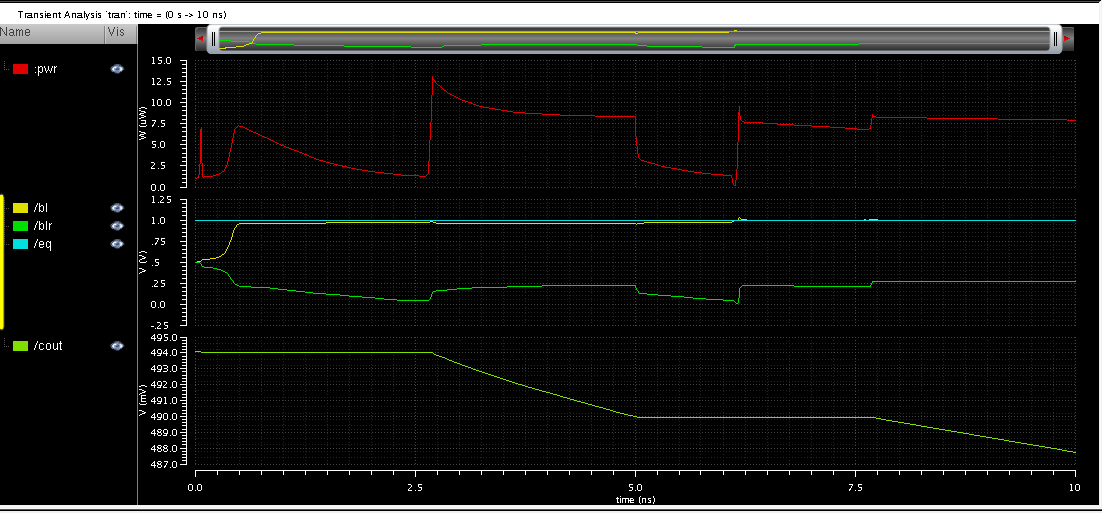
**CHAPTER 7**

**RESULTS AND DISCUSSION**

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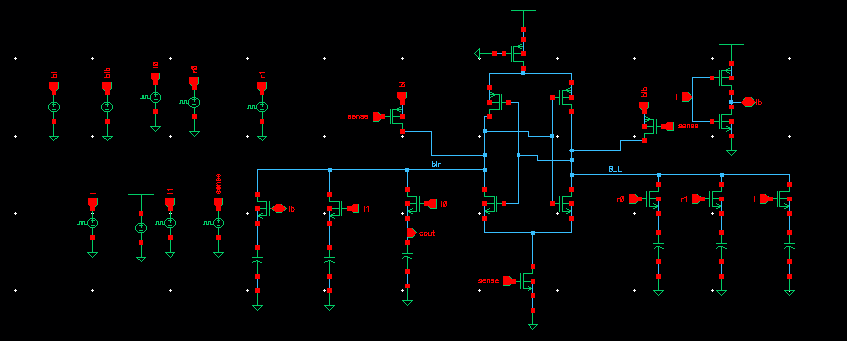
**Fig 33 : SCHEMATIC OF EXISTING METHOD**

This image depicts a schematic of a static random-access memory (SRAM) circuit, including key components such as bitlines, wordlines, and sense amplifiers. The central block shows a 6T SRAM cell array with control signals for reading and writing data. Peripheral circuitry on the right includes sense amplifiers and precharge logic for data sensing and stability.

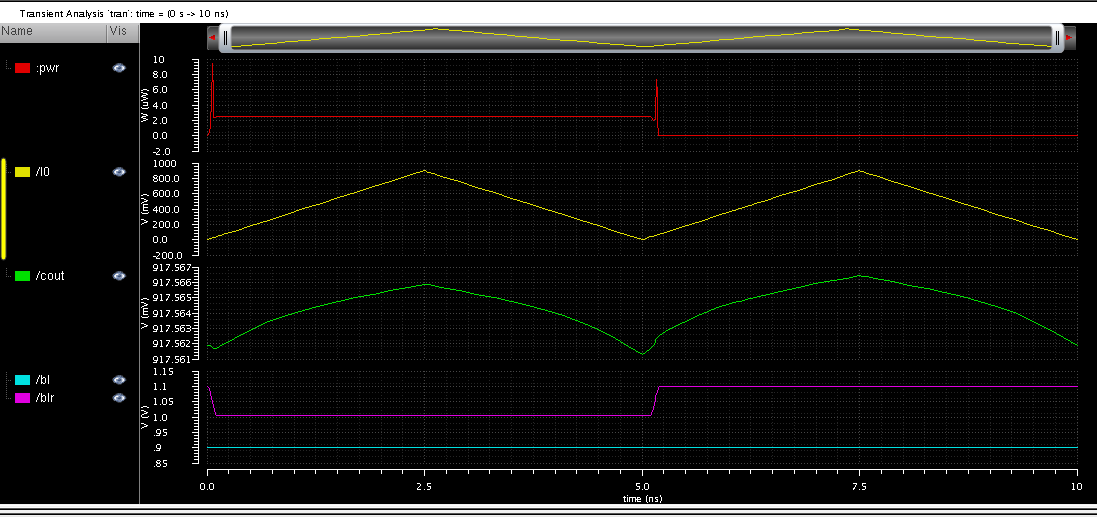
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**Fig 34**: **WAVEFORM OF EXISTING METHOD**

This waveform represents a transient analysis of an SRAM cell's read or write operation over a 10 ns time window. The signals include bitlines (bl, blr), equalization control (eq), and cell output (cout), indicating dynamic voltage changes. The red pwr signal shows power variations, likely corresponding to switching events in the memory array.



**Fig 35: Schematic of Extension DRAM sense amplifier**

Schematic illustrates a simplified single-bit SRAM read circuit with differential bitlines (BL, BLr) and sense amplifier components. The 6T SRAM cell in the center connects to the wordline and bitlines for data access. Peripheral transistors manage sensing (sense) and control signals (pre, sensea) to enable stable and accurate data readout.

**Fig 36**: **Waveform of Extension DRAM Sense amplifier**

Image presents the transient simulation of an SRAM read operation across a 10 ns window. The power signal (pwr) remains steady, with brief switching observed mid-cycle. Input signal /I0 triggers the read operation, resulting in a corresponding change in the output /cout. The bitlines /bl and /blr exhibit minimal variation, indicating a stable and successful read process.

This graph shows the results of a **transient analysis simulation** of a digital circuit, likely related to SRAM (Static Random Access Memory) or a similar memory cell. The simulation tracks how various signals change over time (from 0 to 10 nanoseconds).

**Signal Breakdown**

1. **pwr (Red Line)**
   * Represents the power supply voltage (V<sub>DD</sub>).
   * Remains constant except for a brief dip or spike, possibly indicating a switching event or a momentary current draw.
2. **/I0 (Yellow Line)**
   * Likely an input or control signal, possibly a word line or a data line..
3. **/cout (Green Line)**
   * Represents an output node or a sense amplifier output.
4. **bl (Purple Line) and /blr (Cyan Line)**

* These are likely the **bit line** (/bl) and **bit line bar** (/blr) signals in an SRAM cell.

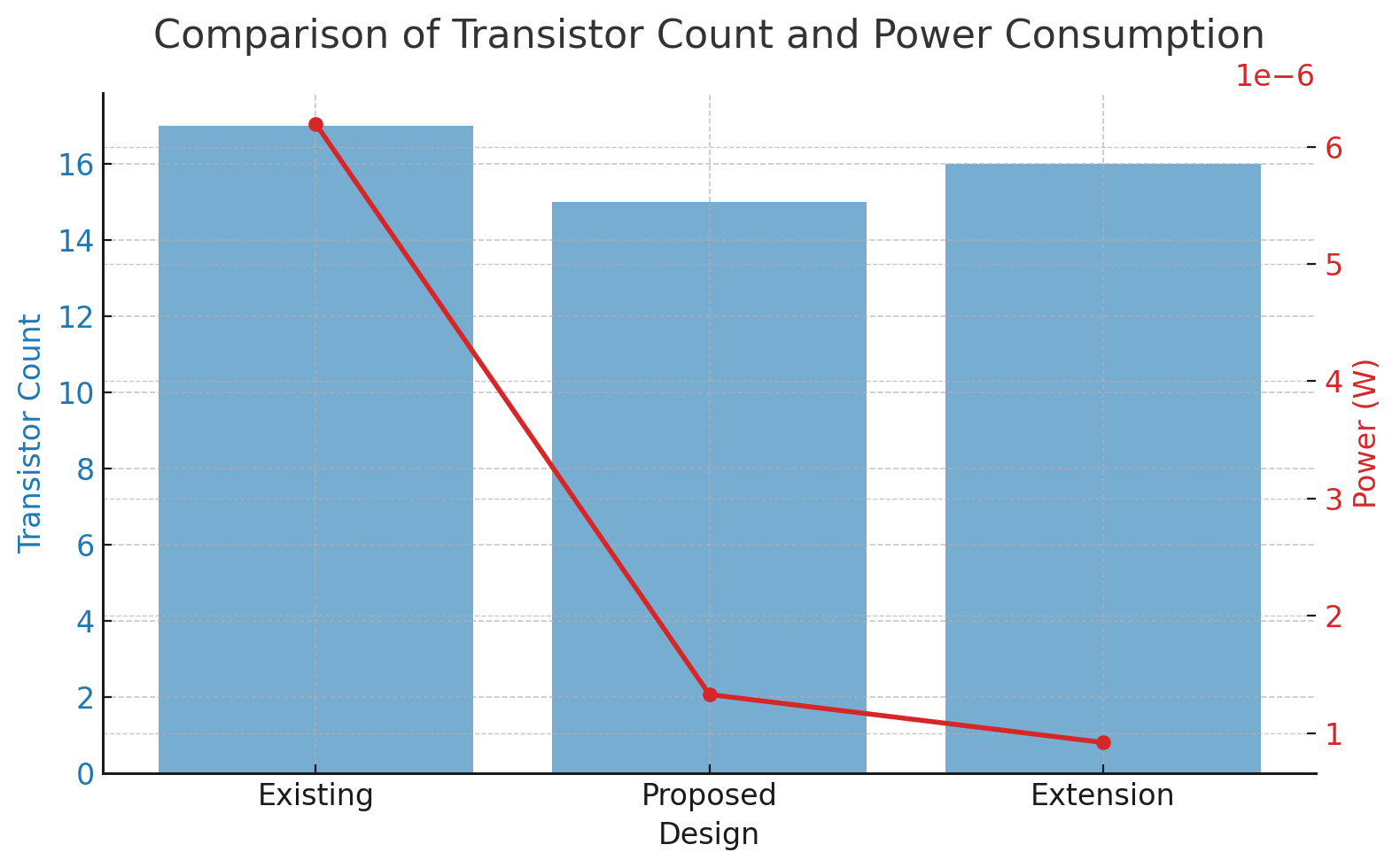
**Key Observations**

* **Transient Behavior:**  
  The signals do not transition instantaneously. Instead, there are gradual changes (ramps) and finite rise/fall times, which are typical in real circuits due to capacitance and resistance.
* **Switching Event:**  
  At around 5 ns, there is a noticeable change in several signals (/bl jumps, /cout and /I0 peak and start to fall, and there’s a brief disturbance in pwr). This likely corresponds to a **read or write operation** in the memory cell.
* **Power Supply Stability:**  
  The power supply (pwr) is mostly stable, with only a minor disturbance during the switching event, indicating good power integrity.
* **Bit Line Dynamics:**  
  The sharp change in /bl and the stability of /blr are characteristic of differential sensing in

SRAM, where only one bit line changes during a read/write operation.

**COMPARISION TABLE 1**

|  |  |  |
| --- | --- | --- |
|  | AREA(Transistors count) | Power (w) |
| Existing | 17 | 6.195 uw |
| Proposed | 15 | 1.328 uw |
| Extension | 16 | 919.2 nW |



**Fig 37 : Graph Representation of Transistor count vs Power consumption**

The comparative analysis of DRAM designs—Existing, Proposed, and Extension—reveals substantial improvements in both area (transistor count) and power consumption. The Existing design consists of 17 transistors and consumes 6.195 µW of power. The Proposed model reduces the transistor count to 15 and achieves a significantly lower power consumption of 1.328 µW. The Extension design, while slightly increasing the transistor count to 16, further optimizes power usage, bringing it down to 919.2 nW. This clearly demonstrates the effectiveness of design modifications in achieving power-efficient and area-optimized SRAM architectures.

**Key Observations:**

* **Existing Design**: 17 transistors, 6.195 µW power consumption.
* **Proposed Design**: 15 transistors, 1.328 µW power consumption (≈78.6% power reduction).
* **Extension Design**: 16 transistors, 919.2 nW power consumption (≈85.2% power reduction).
* The proposed and extension designs show significant efficiency gains while minimizing area overhead.
* These results suggest suitability for low-power and compact memory applications.

COMPARISON TABLE OF DELAY

|  |  |
| --- | --- |
|  | DELAY |
| Existing | 331.4 |
| Proposed | 39.51 |
| Extension | 21.66 |

The existing design experiences a delay of 331.4 ps, which affects overall performance. By implementing the proposed method, the delay is significantly reduced to 39.51 ps due to improved circuit efficiency and optimized signal propagation. Furthermore, the extended version enhances performance even further, bringing the delay down to 21.66 ps by incorporating advanced techniques that minimize transition time and improve response speed. This substantialreduction in delay makes the extended design highly efficient for high-speed applications.

**CHAPTER-8**

**CONCLUSION**

The proposed study evaluates the power consumption during read operations in the open bit architecture technique of DRAM sense amplifiers. It reveals that the power consumption in the proposed technique of DRAM sense amplifier using FSPA-VLSA is roughly 81% less than that of the open bit architecture of DRAM sense amplifier using a basic latch type sense amplifier. This reduction is attributed to the application of the same pulse to all circuit inputs. The PMOS transistor is active and the NMOS transistor is inactive for half the interval of time, followed by the NMOS transistor being active and the PMOS transistor inactive for the rest of the simulation time. Consequently, the circuit spends most of its time in a cut-off state, either due to the NMOS or PMOS, which results in a reduced overall power consumption.

**FUTURE SCOPE**

the broader scope of core electronics and communication engineering (ECE), the implementation of such power-efficient circuits can significantly benefit domains like embedded systems, IoT devices, and mobile computing. These areas demand compact, high-performance, and energy-aware hardware solutions. The integration of FSPA-VLSA into these platforms not only supports sustainable and portable device development but also aligns with the future direction of ubiquitous computing and wearable technologies. As such, this technique is not only a hardware innovation but also a stepping stone toward more intelligent, autonomous, and energy-conscious electronic systems.

**Embedded Systems**:

* Used in automotive ECUs (Engine Control Units) and industrial controllers.
* FSPA-VLSA can reduce power in memory access, enhancing system reliability.

**IoT Devices**:

* Deployed in smart home devices and environmental monitoring sensors.
* Enables longer battery life through ultra-low-power memory operation.

**Wearable Technology**:

* Used in smartwatches, fitness bands, and health monitors.
* Supports compact and energy-efficient memory for prolonged device operati

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**PROJECT TITLE:** **DESIGN OF DRAM SENSE AMPLIFIER USING 45NM TECHNOLOGY**

**ABSTRACT:** Power consumption is a critical consideration in the design of memory elements and digital systems within very large scale integration (VLSI) circuits. This study introduces a method for reducing power consumption in DRAM sense amplifiers, termed FSPA-VLSA (Foot Switch PMOS Access Voltage Latch Type Sense Amplifier). By implementing this technique within the open bit architecture of DRAM Cells during read operations, an approximate 81% reduction in overall power consumption has been achieved. Additionally, this proposed circuit offers advantages for low-power VLSI/ULSI design. The circuit has been successfully designed and implemented using Cadence Virtuoso tools at 45nm technology.

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| Optimized N-Tap FIR Filter for Biomedical Signal Enhancement | **√** | **√** | **√** | **√** | **√** | **√** | **√** | **√** | **√** | **√** | **√** | **√** | **√** | | **√** | **√** | **√** |

**Signature of the Supervisor**

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**APPENDIX – I**

**PUBLICATIONS**

***Paper Id:* 1470**

***SUBMISSION TITLE*: - POWER-EFFICIENT DRAM SENSE AMPLIFIER DESIGN USING POWER GATING IN 45NM TECHNOLOGY**

****

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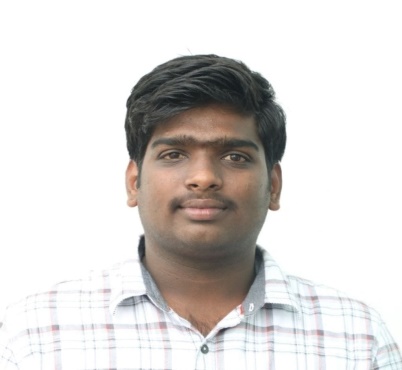
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